University of California, Davis
Society of Manufacturing Engineers at UC Davis

EEC 110A*	Electronics Circuits I	Unofficial

Mock Unofficial Practice Final Exam Solution

*Disclaimer: This document is the solutions to a sample final exam of an Electronics Circuits I midterm. It is a mock exam and does not necessarily reflect the format—in the length of the exam, content covered, the protocol, and other aspects—of an actual final exam of EEC 110A in University of California, Davis. However, this covers multiple topics that seems to be a complete agenda of EEC 110A and this document is an attempt to give students extra practice. The problems in this document are written entirely by the author. Any similarity, either in part or in whole, is a complete coincidence. If an error is caught, or if you have any questions and inquiries, please contact the author at mnhyu@ucdavis.edu.

A calculator is not encouraged where not needed. Scoring distribution for each question is not provided as it discourages students from judging the importance of a topic over another.

This solution has fourteen (14) pages, including this front cover page and the topology sheet.

Question 1) Short Response Questions	
Question 2) Diode Circuit Applications - Limiters	
Question 3) BJT Topology and Biasing	
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Question 6) Feedback	

Note: Nodal V_{IN} in the schematics represent small signal AC inputs.

1) Short Response Questions

Explain your claim for each in one sentence.

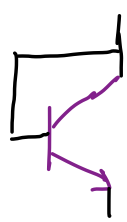
a) True or False: the unit for $\mu_N C_{OX}(W/L)*V_{TH}$ is Ω, resistance.

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})^2$$

$$[A] \propto \left\{\mu_n C_{ox}\frac{W}{L}\right\}[V]^2$$

$$[A/V] \propto \left\{\mu_n C_{ox}\frac{W}{L}\right\}[V] \propto [\mho] \equiv [\Omega]^{-1}$$

b) To “diode-connect” a BJT, what two terminals of a BJT should an engineer short together? Recall that diode-connecting a BJT directly puts the transistor at the edge of saturation.



FAR: $V_{BC} < 0$

So edge: $V_{BC} = 0$

So short B & C

c) True or False: for an emitter follower, the absolute voltage gain is always less than or equal to one, that is, $|A_V| \leq 1$.

$$|A_v| = \frac{R_C||R_o}{1/g_m + R_C||R_o} \overset{?}{<} 1$$

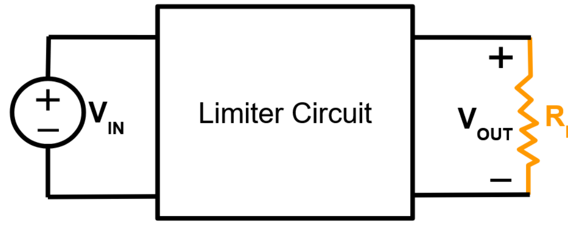
$$\cancel{R_C||R_o} \overset{?}{<} \frac{1}{g_m} + \cancel{R_C||R_o}$$

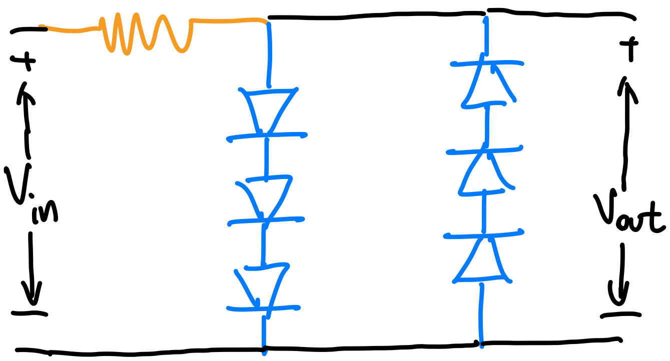
$$0 \overset{?}{<} \frac{1}{g_m} \quad \text{Yes!}$$

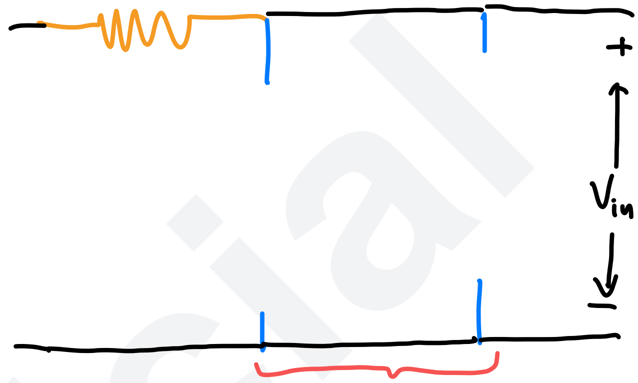
Also, EFs are not meant to be amplifiers; they are buffers.

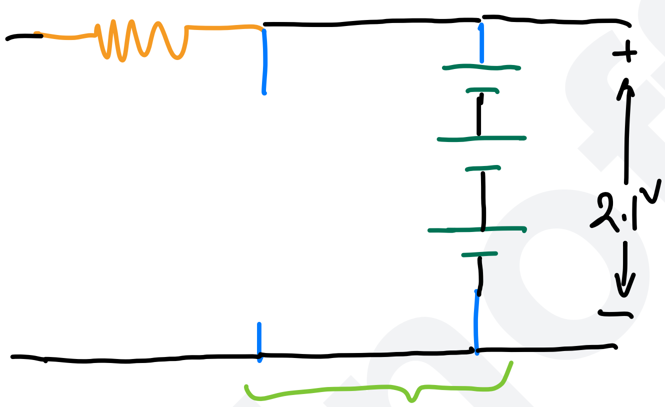
2) Diode Circuit Applications - Limiters

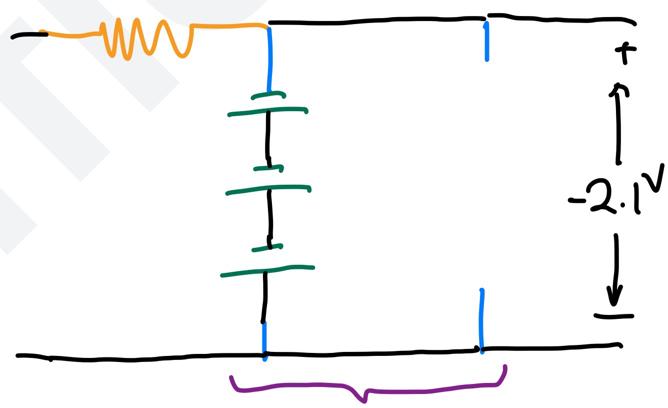
Using diodes with $V_{D,ON} = 0.7V$ and a 10 Ω resistor, engineer a limiter so V_{OUT} swings between $\pm 2.1^V$. If $V_{IN} = 3\sin(2t)$, sketch V_{IN} and V_{OUT} over time from $0s \leq t \leq 1s$ on the same graph.

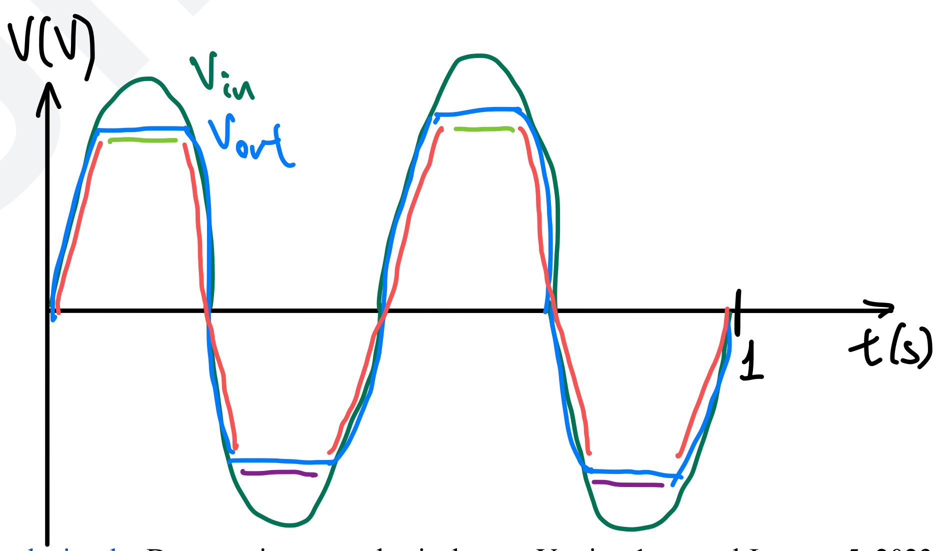










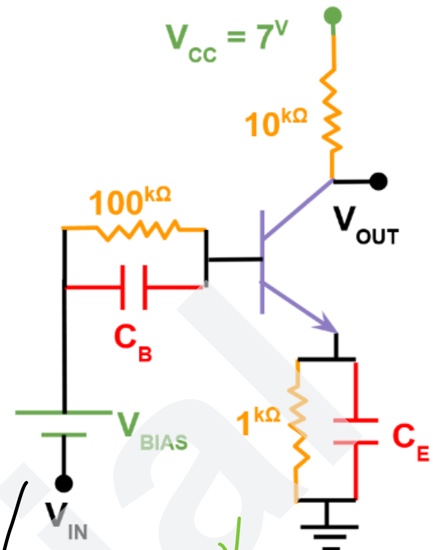


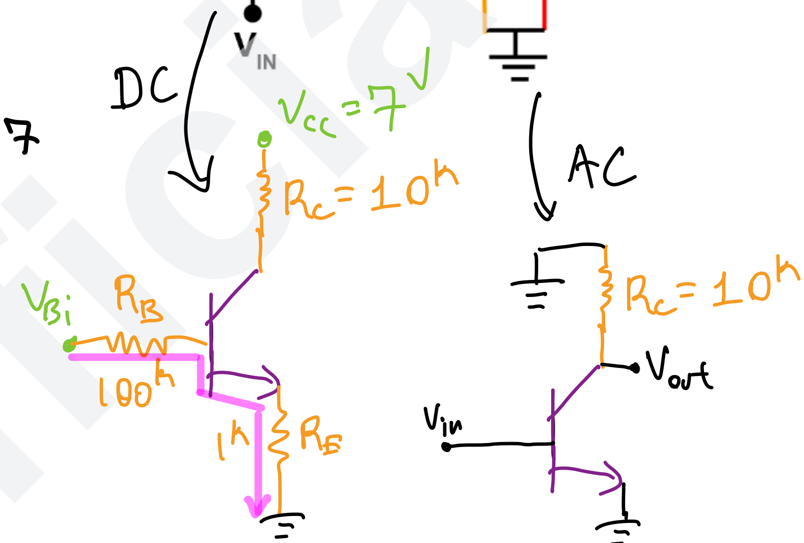
3) BJT Topology and Biasing

The BJT here has $V_A = 5.722^V$, $V_{BE,ON} = 0.7V$, $\beta = 99$.

a) Find V_{Bias} so that the BJT is operating at the boundary of saturation and forward active region.

b) Using your V_{Bias} from part a), find $A_V = V_{OUT}/V_{IN}$. Both capacitors are very large and short for AC signals.





$$V_{Bi} - R_B i_B - V_{BEON} - i_B(\beta+1)R_E = 0$$

KVL: $V_{Bi} = i_B(R_B + (\beta+1)R_E) + V_{BEON}$

$$= i_B(100^k + 100^k) + .7 = 200^k i_B + .7$$

$\xrightarrow{}$ FAR $\quad i_B = (V_{Bi} - .7)/200^k$ ①

$$V_{BC} < 0$$

$$V_{BC} = \underbrace{V_{Bi} - R_B i_B}_{V_B} - \underbrace{(V_{cc} - R_c i_B \beta)}_{V_C}$$

$$V_{Bi} + i_B(R_c\beta - R_B) < V_{cc}$$

$$V_{Bi} + \frac{(V_{Bi} - .7)}{200^k}(990-100)^k < 7$$

$$V_{Bi} \lesssim 1.856^V$$

At $V_{Bi} = 1.856^V$, $i_c \simeq 572.202\,\mu A$ & if $V_T = 25^{mV}$, $g_m = 22.888^{m℧}$

$$A_v = -g_m(R_c \| r_o) = -22.888^m\left(10^k \,\Big\|\, \frac{5.722^V}{572.2^{\mu A}}\right)$$

$$= -22.888^{m℧} \times 5^{k\Omega}$$

$$A_v = -114.44$$

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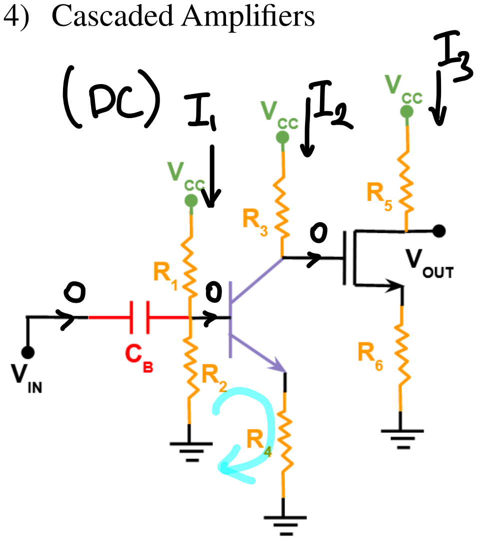
4) Cascaded Amplifiers



The BJT here has $V_A = \infty^V$, $V_{BE,ON} = 0.7^V$, $\beta = \infty$, $V_T = 25^{mV}$. The MOS here has $\lambda = 0$, $V_{TH} = 0.4^V$, $\mu_N C_{OX} = 200\ \mu A \cdot V^{-2}$, and L = 45µm. C_B is very large and $V_{CC} = 8^V$. Engineer this cascaded amplifier by choosing all six resistor values and the width of the MOS to meet all conditions. You are also allowed a large capacitor to short a resistor in AC. If you choose, indicate which one resistor. Conditions:

- $V_{OUT}/V_{IN} \geq 300$.
- $(W/L)_N$ should realistically be at least 20.
- To protect each transistor, neither stage should have an absolute gain of higher than 30.
- Maximum DC power consumption is 1 mW.

There are many possible ways to tackle this problem. This solution is one of the very many.

Let I_1 be the current flowing through R_1 and R_2. Taking the KVL of the far left branch in DC, and since we can neglect the base current of the BJT, we have a simple voltage divider.

$$I_1 = \frac{V_{DD}}{R_1 + R_2} = \frac{8}{R_1 + R_2}$$

We should decide R_1 and R_2 based on how much current we can have going through them. Since there are three DC currents in this circuit, let's assume that we would like a third the current budget for I_1. We do not have to abide by this for the other two DC currents, but it is a good measure to decide the first two resistor values.

$$I_1 V_{DD} \cong \frac{P_{bank}}{3} \rightarrow I_1 \cong \frac{1^{mW}}{3 \cdot 8^V} \simeq \frac{8^V}{R_1 + R_2}, \text{ so}$$

$$192^{k\Omega} \simeq R_1 + R_2 \quad (1)$$

The voltage drop across R_2 should be at least 700mV to accommodate for $V_{BE,ON}$. Let's be safe and have that voltage drop to be 800mV.

$$I_1 R_2 = 0.8^V$$

Since 0.8V is 10% of V_{CC},

$$\frac{R_2}{R_1 + R_2} = 0.1 \quad ②$$

To satisfy equation 1 and 2 simultaneously, R_1 = 172.8kΩ and R_2 = 19.2kΩ, and that also makes $I_1 \simeq$ 41.67 μA. Now, we should find the collector current (also the emitter current and let it be I_2) to find the appropriate bias points for the BJT. Notice that we would have to choose R_4, so we have some freedom here as well. Per KVL around R_2, V_{BE}, and R_4,

$$I_1 R_2 = V_{BE} + I_2 R_4$$

Assuming that the BJT is in the FAR (we will check this later), V_{BE} = 0.7V. Let's arbitrarily choose R_4 to be 10kΩ, which seems reasonable (but if it's not, we can change it later).

$$\frac{41.67\mu A(19.2k\Omega) - 0.7}{10k\Omega} = 10\mu A = I_2$$

We are allowed to have a gain of -30 in a given stage. Let's maximize that here. Using the BJT stage is a common collector stage with a gain, we can determine R_3

$$-\frac{R_C}{1/g_m + R_E} = -\frac{R_3}{1/g_{mQ} + R_4} = \frac{-R_3}{25mV/10\mu A + 10k\Omega} = -30$$

That makes R_3 = 375kΩ. Now, to verify that we are in the forward active region, so all our equations we have used are valid, we would want to make sure that $V_{BC} < 0$.

$$V_{BC} = V_{DD}\frac{R_2}{R_1 + R_2} - V_{DD} + R_3 I_2 < 0$$

$$8(0.1) - 8 + 375(0.01) = -3.45 < 0$$

Let's check our power budget so far.

$$P_{(1+2)} = V_{DD}(I_1 + I_2) = 8^V(41.67^{\mu A} + 10^{\mu A}) = 413.33\mu W$$

We still have 586.67 µA left in our bank, so the drain current of the MOS would have to be at most 73.33 µA. Remember, our goal now is to achieve at least -10 for the MOS stage to have an ultimate gain of 300. We should be cautious here, because it is harder to achieve a gain of larger than one if we have a common source with degeneration, so we should short out the degenerating resistor, R_6, using a large capacitor. With that, our gain for stage 2 is now simply $A_V = -g_{mM} R_5$ where $g_{mM} = \sqrt{2\mu_N C_{ox} \frac{W}{L} I_D}$. So we simply have to decide our size ratio and drain current from that. We have to make sure that the MOS is in saturation, and we should check to see what our limit is

$$V_{GD} < V_{TH} \rightarrow V_G - V_D = 4.25 - (8 - I_D R_4) < 0.4, \text{ so}$$

$$I_D R_5 < 4.15 \quad (3)$$

If we aim to have a gain of -10, then we can change the condition of equation 3 to not include R_5.

$$-10 = -R_5\sqrt{2\mu_n C_{ox} I_D W/L}, \qquad \frac{10\sqrt{I_D}}{\sqrt{2\mu_n C_{ox} W/L}} < 4.15 \quad (4)$$

With our maximum of I_D = 73.33 µA and minimum W/L = 20, equation 4 is satisfied regardless of what size and drain current we choose and we would remain in saturation. Let's choose a small I_D to minimize power usage, and I_D = 10 µA and W/L as a minimum of 20 (so W = 900µm), and pair this with a R_5 = 50kΩ. This gives us a -14.14 gain, and the overall gain would be 424.3. We still need to find R_6 that yields such drain current.

$$I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})^2$$

$$10 = \frac{1}{2} 200 \times 20 (V_{GS} - 0.4)^2$$

$$V_{GS} \approx 470.7\text{mV}$$

$$V_{GS} = V_G - I_D R_6$$

$$.4707 = 4.25 - 10\mu A \times R_6 \rightarrow R_6 \simeq 458^{k\Omega}$$

which is shorted in AC by a parallel capacitor. In conclusion,

$R_1 = 172.8^{k\Omega}$ $\quad R_4 = 10^{k\Omega}$ $\quad$ Choose large C in parallel w/ R_6

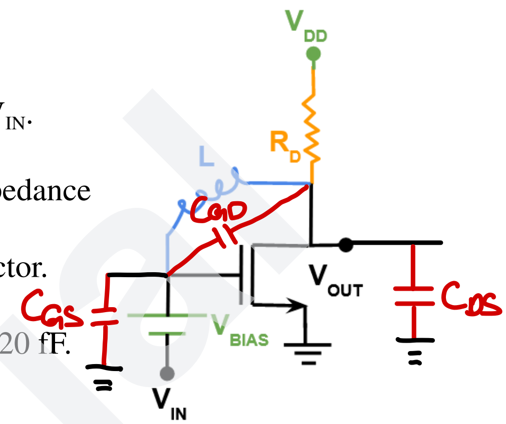
$R_2 = 19.2^{k\Omega}$ $\quad R_5 = 50^{k\Omega}$ $\quad W/L = 900\mu m / 45\mu m = 20$

$R_3 = 375^{k\Omega}$ $\quad R_6 = 458^{k\Omega}$

And this gives us a gain of 424.3 and consumes 493.33 µW in DC.

5) High Frequency Analysis of MOS Amplifiers

Given the amplifier below, where $\lambda = 0$, $V_{TH} = 0.4^V$, $\mu_N C_{OX} = 400\ \mu A{*}V^{-2}$, $W/L = 30$, $V_{BIAS} = 0.5^V$, $R_D = 50^{k\Omega}$, and an L that (for part b and d) is super large so any AC signal will open circuit it,



a) Find the drain current in DC.

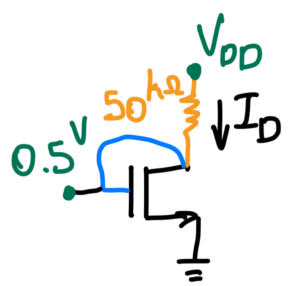
b) From the small signal model, find the low frequency gain V_{OUT}/V_{IN}.

c) Using your gain from part b), find the exact output and input impedance in terms of L, C_{GD}, C_{DS}, C_{GS}, and ω. Do not open circuit the inductor.

$C_{GD} = 5fF \quad C_{GS} = 10fF$

d) Approximate the output pole frequency, if $4C_{GD} = 2C_{GS} = C_{DS} = 20$ fF.

DC: (L is short ckt)



$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2$$

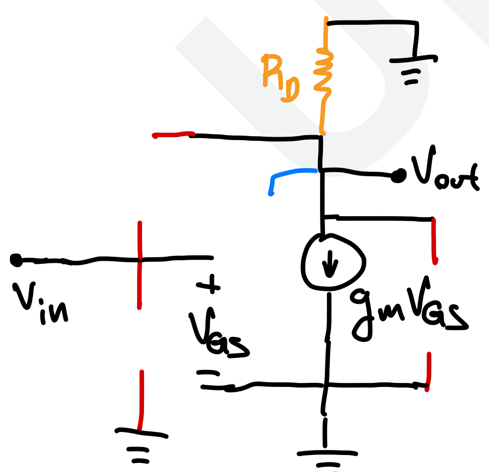
$$= \frac{1}{2}\,400 \times 30\,(0.5 - 0.4)^2 = 60\mu A = I_D$$

FAR? $V_{GD} \overset{?}{<} V_{TH}$

$0 < 0.4$ Yes

$$g_m = \sqrt{2\mu_n C_{ox}\frac{W}{L} I_D} = \sqrt{2 \times 400\mu \times 30 \times 60\mu} = 1.2m℧$$

AC: (L is open, freq is low enough to have small caps be open



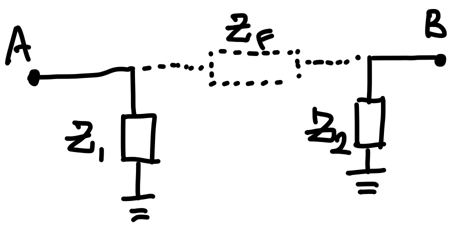
$V_{in} = V_{GS}$

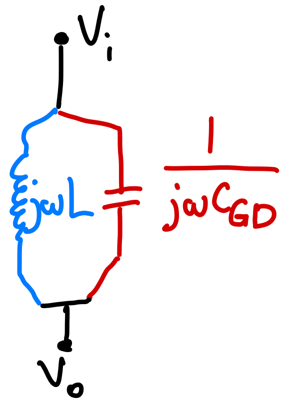
$V_{out} = -R_D g_m V_{GS}$

$A_V = -g_m R_D$

$-g_m R_D = -60 = A_V$

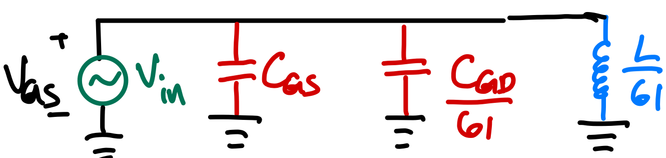
Miller's



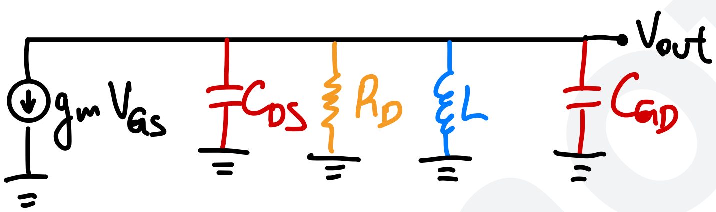


$$Z_1 = Z_F\left(1+\frac{V_B}{V_A}\right)^{-1}$$
$$Z_2 = Z_F\left(1+\frac{V_A}{V_B}\right)^{-1}$$

$$\frac{1}{j\omega C_1} = \frac{(1+60)^{-1}}{j\omega C_{GD}} \qquad \frac{1}{j\omega C_2} = \frac{(1+1/60)^{-1}}{j\omega C_{GD}}$$
$$C_1 = \frac{C_{GD}}{61} \qquad C_2 \approx C_{GD}$$
$$j\omega L_1 = \frac{j\omega L}{1+60} \qquad j\omega L_2 = \frac{j\omega L}{1+1/60}$$
$$L_1 = \frac{L}{61} \qquad L_2 \approx L$$

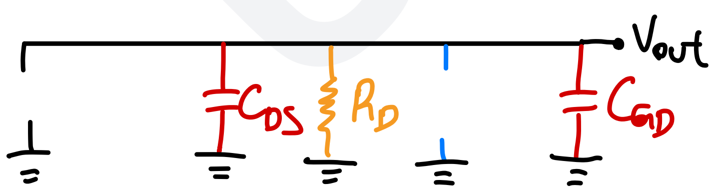


$$Z_{in} = \frac{-j}{\omega\left(C_{GS}+\frac{C_{GD}}{61}\right)} \,\Big|\Big|\, \frac{j\omega L}{61}$$



$$Z_{out} = j\omega L \,\Big|\Big|\, \frac{-j}{\omega(C_{GD}+C_{DS})} \,\Big|\Big|\, 50^k$$

Output pole



$$\omega_{out} \approx \frac{1}{R_D(C_{DS}+C_{GD})}$$
$$\approx \frac{1}{50e3 \times 25e{-15}} \approx 800^{Mrad/s}$$
$$f_{out} = \frac{\omega_{out}}{2\pi} \approx 127.32\ MHz$$

6) Feedback

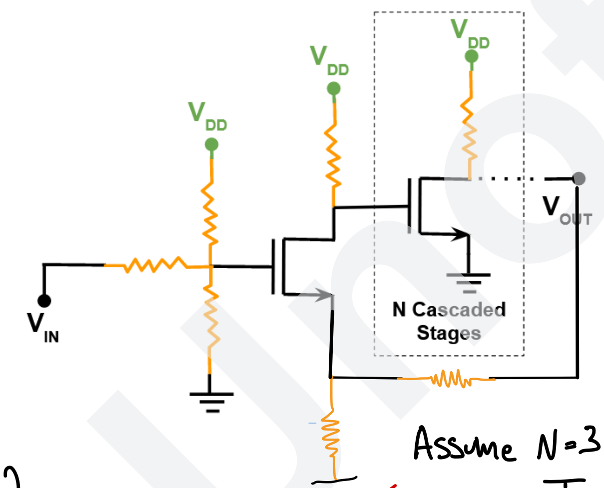
For a negative feedback amplifier with forward gain of A and feedback gain of β,

$$A(s) = \frac{10^{13}}{(s+T_X)(s+10)(s+10^3)(s+10^5)}.$$

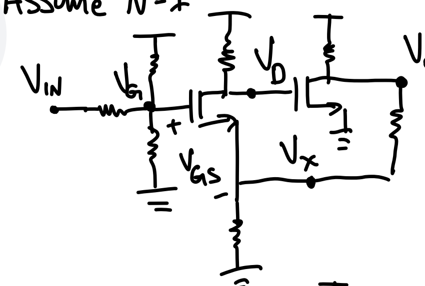
Find phase margin and comment on stability for each T_X and β combination below. If the open loop system is unstable, find an extra factor, K, of gain to A(s) so the open loop system oscillates.

	T_X	β	PM (°) - Stable?	Open Loop Stability	K (if applicable)
a)	1	1	22.5° unstable	Unstable	0.1
b)	10	0.1	0° unstable	Unstable	0.1
c)	0	0.01	22.5° stable	Unstable	0.1

d) Given a general amplifier (not necessarily part a-c), complete the circuit using general resistors to implement negative feedback. What (kind of) value should N be?



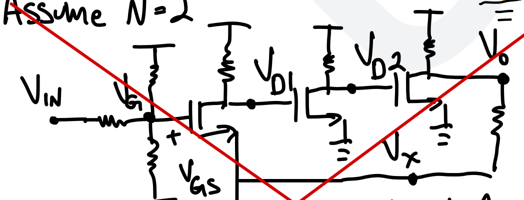
Assume N=1



If $V_{in}\uparrow$, $V_G\uparrow$, $I_{D1}\uparrow$ b/c $I_D \propto (V_{GS}-V_{TH})^2$

$\therefore V_D\downarrow$, $I_{D2}\downarrow$, $V_{out}\uparrow$, $V_x\uparrow$, $I_{D1}\downarrow$ NFB!

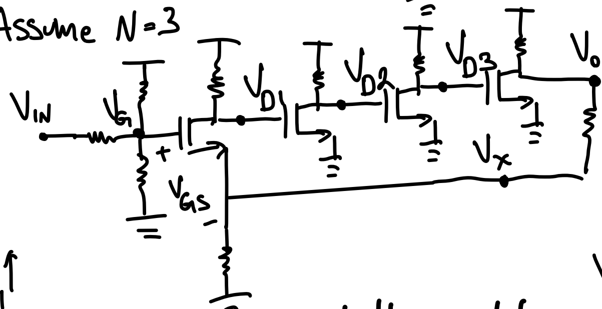
~~Assume N=2~~



~~If $V_{in}\uparrow$, $V_G\uparrow$, $I_{D1}\uparrow$~~

~~$\therefore V_{D1}\downarrow$, $I_{D2}\downarrow$, $V_{D2}\uparrow$, $I_{D3}\uparrow$, $V_o\downarrow$, $V_x\downarrow$, $I_{D1}\uparrow\uparrow$ PFB!~~

Assume N=3



If $V_{in}\uparrow$, $V_G\uparrow$, $I_{D1}\uparrow$

$\therefore V_{D1}\downarrow$, $I_{D2}\downarrow$, $V_{D2}\uparrow$, $I_{D3}\uparrow$, $V_{D3}\downarrow$, $I_{D4}\downarrow$, $V_{out}\uparrow$

$V_x\uparrow$, $I_{D1}\downarrow$ NFB!

and the pattern continues

N should be odd

d) $T_x = 1$ & $\beta = 1$

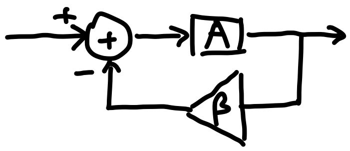
Osc: $|\beta A| = +1$

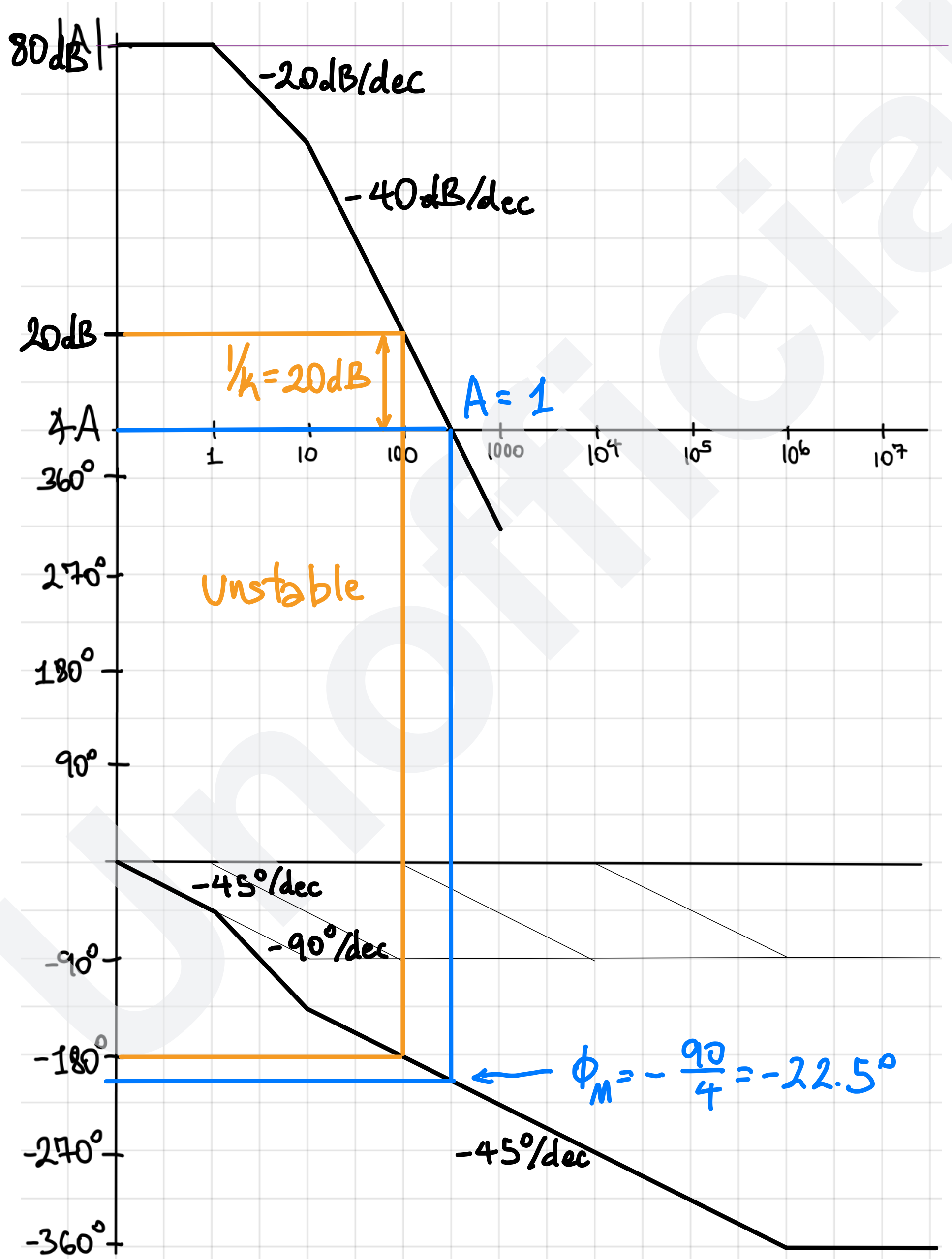
$|A| = 1$

$$A(s) = \frac{10^{13}}{(s+T_x)(s+10)(s+10^3)(s+10^5)}$$

$$= \frac{10^{13}}{(s+1)\left(\frac{s}{10}+1\right)10\left(\frac{s}{10^3}+1\right)10^3\left(\frac{s}{10^5}+1\right)10^5}$$

$$= \frac{10^4\ (80\text{dB})}{(s+1)\left(\frac{s}{10}+1\right)\left(\frac{s}{10^3}+1\right)\left(\frac{s}{10^5}+1\right)}$$





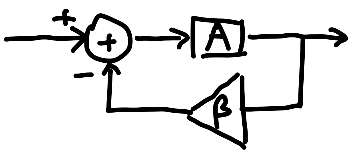
b) $T_x = 10$ & $\beta = .1$

$$A(s) = \frac{10^{13}}{(s+T_x)(s+10)(s+10^3)(s+10^5)}$$

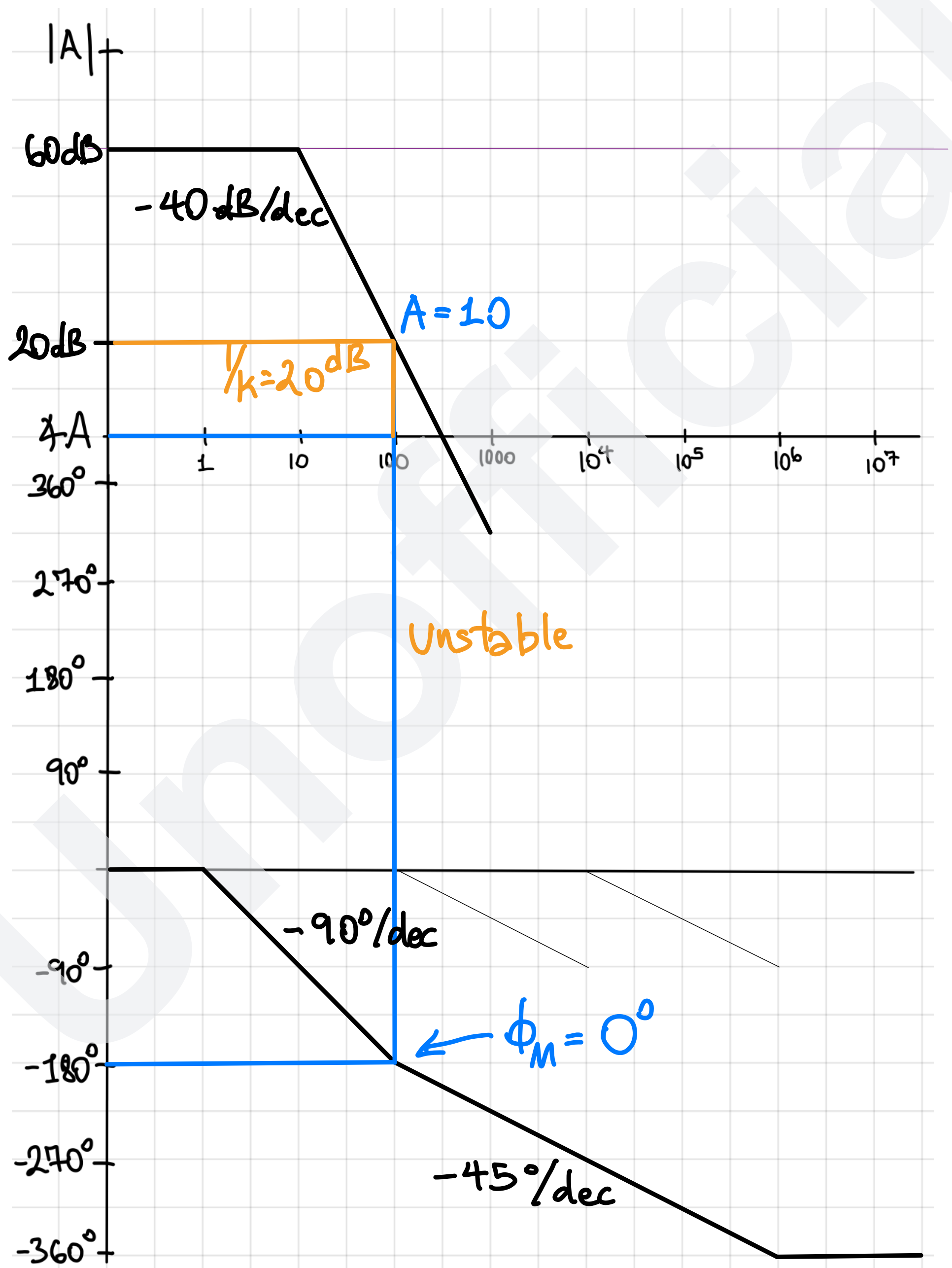
Osc: $|\beta A| = +1$

$|A| = 10$

$$= \frac{10^{13}}{\left(\frac{s}{10}+1\right)^2 10^2 \left(\frac{s}{10^3}+1\right)10^3\left(\frac{s}{10^5}+1\right)10^5}$$



$$= \frac{10^3\ (60dB)}{\left(\frac{s}{10}+1\right)^2\left(\frac{s}{10^3}+1\right)\left(\frac{s}{10^5}+1\right)}$$



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c) $T_x = 0$ & $\beta = .01$

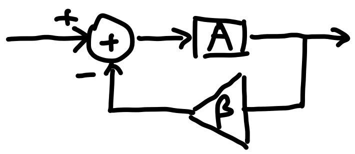
Osc: $|\beta A| = +1$

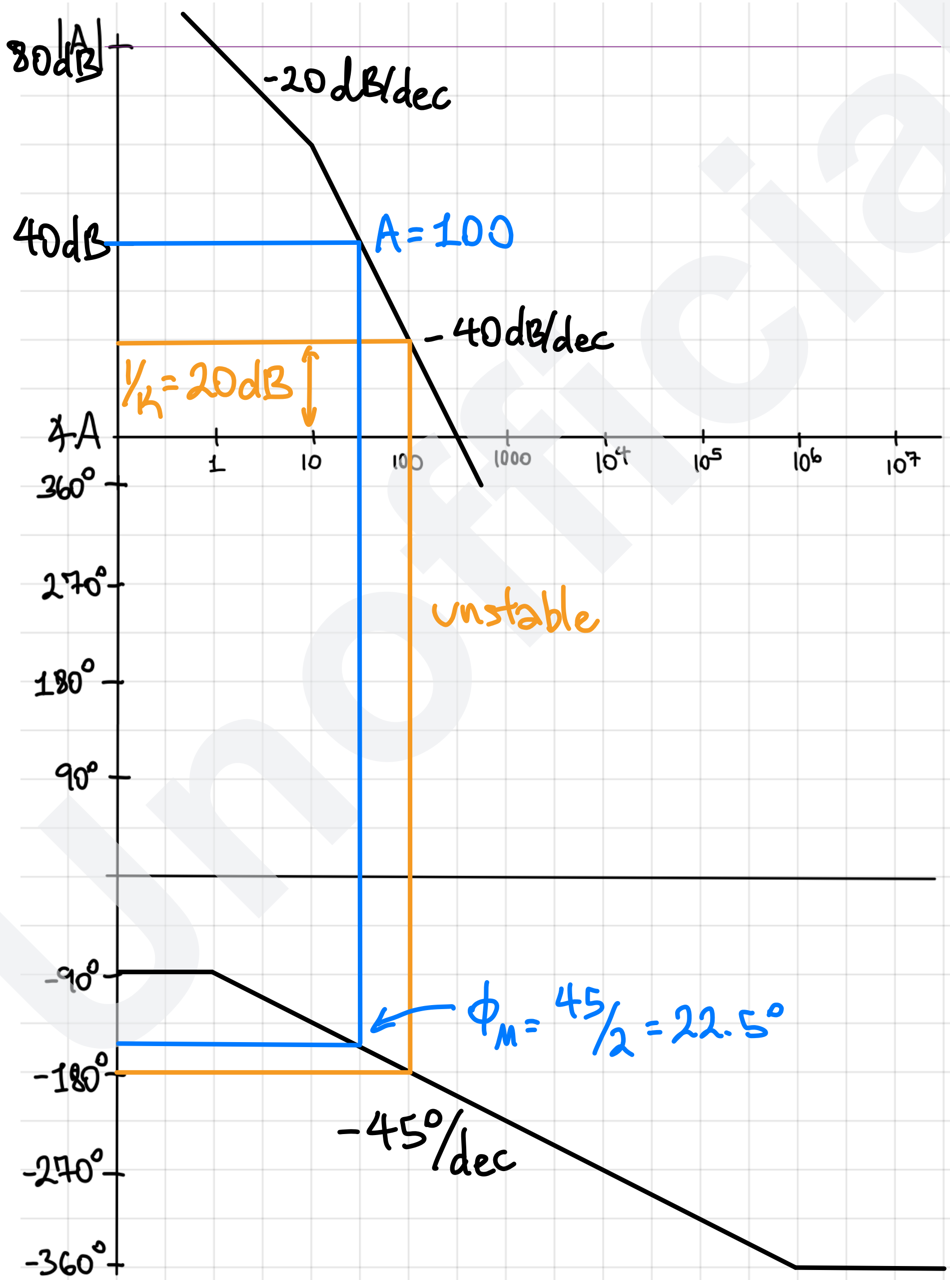
$|A| = 100$

$$A(s) = \frac{10^{13}}{(s+T_x)(s+10)(s+10^3)(s+10^5)}$$

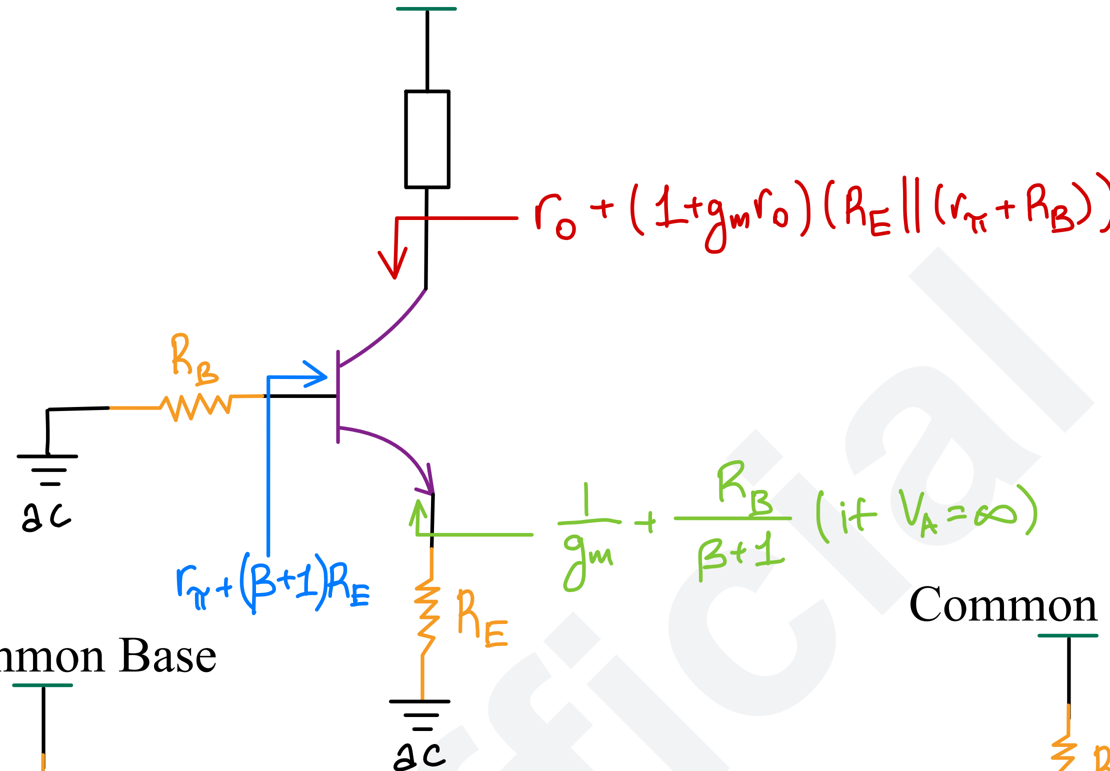
$$= \frac{10^{13}}{s\left(\frac{s}{10}+1\right)10\left(\frac{s}{10^3}+1\right)10^3\left(\frac{s}{10^5}+1\right)10^5}$$

$$= \frac{10^4 \ (80dB)}{s\left(\frac{s}{10}+1\right)\left(\frac{s}{10^3}+1\right)\left(\frac{s}{10^5}+1\right)}$$

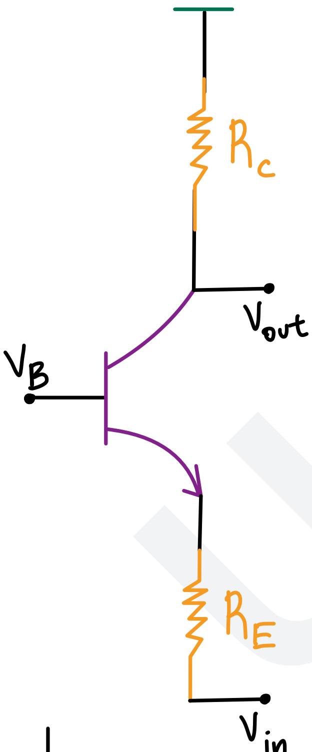




Topology Sheet

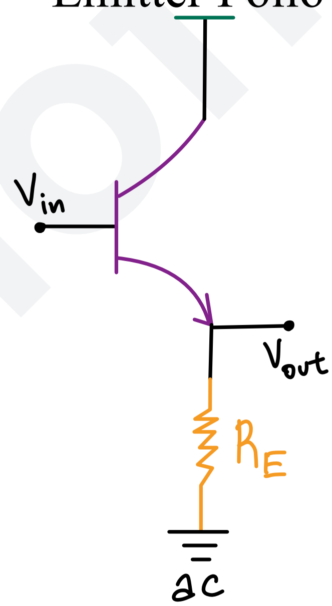


Common Base



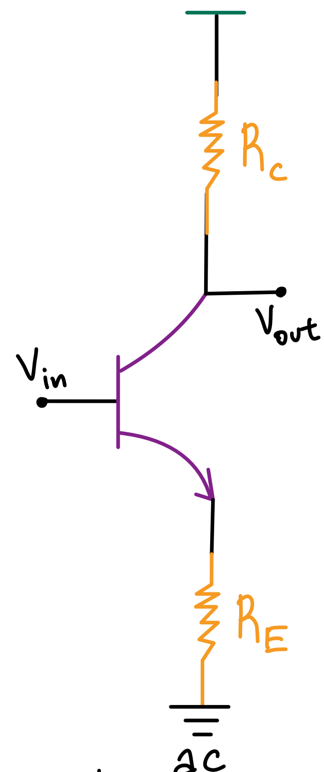
$$\left.V_{out}/V_{in}\right|_{V_A=\infty} = \frac{R_C}{\frac{1}{g_m} + R_E}$$

Emitter Follower



$$V_{out}/V_{in} = \frac{R_E \| r_o}{\frac{1}{g_m} + R_E \| r_o}$$

Common Collector



$$\left.V_{out}/V_{in}\right|_{V_A=\infty} = \frac{-R_C}{\frac{1}{g_m} + R_E}$$