University of California, Davis
Society of Manufacturing Engineers at UC Davis

EEC 110A*   Electronics Circuits I   Unofficial

Mock Unofficial Practice Final Exam

*Disclaimer: This document is a sample final exam of an Electronics Circuits I midterm. It is a mock exam and does not necessarily reflect the format—in the length of the exam, content covered, the protocol, and other aspects—of an actual final exam of EEC 110A in University of California, Davis. However, this covers multiple topics that seems to be a complete agenda of EEC 110A and this document is an attempt to give students extra practice. The problems in this document are written entirely by the author. Any similarity, either in part or in whole, is a complete coincidence. If an error is caught, or if you have any questions and inquiries, please contact the author at mnhyu@ucdavis.edu.

A calculator is not encouraged where not needed. Scoring distribution for each question is not provided as it discourages students from judging the importance of a topic over another.

This examination has eight (8) pages, including this front cover page and the topology sheet.

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Note: Nodal V_{IN} in the schematics represent small signal AC inputs.

1) Short Response Questions

Explain your claim for each in one sentence.

a) True or False: the unit for $\mu_N C_{OX}(W/L) \cdot V_{TH}$ is Ω, resistance.

b) To "diode-connect" a BJT, what two terminals of a BJT should an engineer short together? Recall that diode-connecting a BJT directly puts the transistor at the edge of saturation.

c) True or False: for an emitter follower, the absolute voltage gain is always less than one, that is, $|A_V| < 1$.

2) Diode Circuit Applications - Limiters

Using diodes with $V_{D,ON} = 0.7V$ and a 10 Ω resistor, engineer a limiter so V_{OUT} swings between $\pm 2.1^V$. If $V_{IN} = 3\sin(2t)$, sketch V_{IN} and V_{OUT} over time from $0s \leq t \leq 1s$ on the same graph.
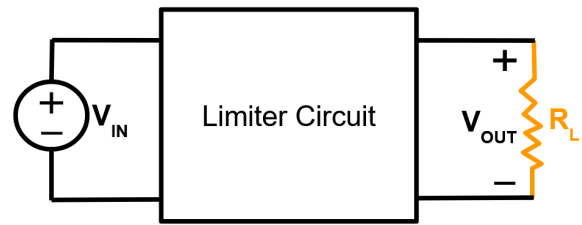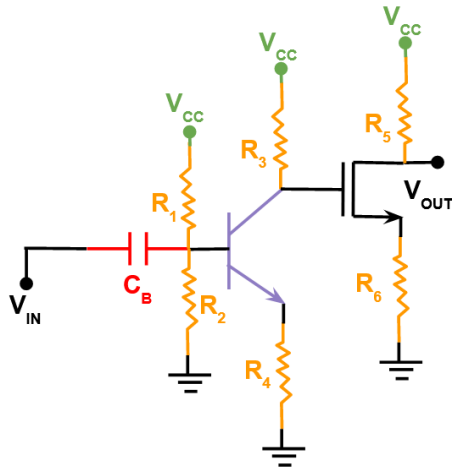
3) BJT Topology and Biasing

The BJT here has $V_A = 5.722^V$, $V_{BE.ON} = 0.7V$, $\beta = 99$.

a) Find V_{Bias} so that the BJT is operating at the boundary of saturation and forward active region.

b) Using your V_{Bias} from part a), find $A_V = V_{OUT}/V_{IN}$. Both capacitors are very large and short for AC signals.
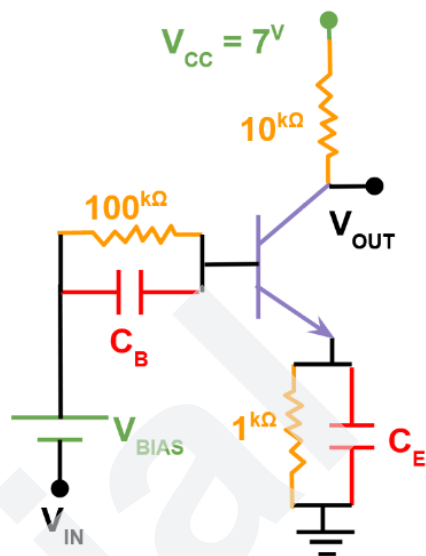
4) Cascaded Amplifiers

The BJT here has $V_A = \infty^V$, $V_{BE.ON} = 0.7^V$, $\beta = \infty$, $V_T = 25^{mV}$. The MOS here has $\lambda = 0$, $V_{TH} = 0.4^V$, $\mu_N C_{OX} = 200 \ \mu A*V^{-2}$, and $L = 45\mu m$. C_B is very large and $V_{CC} = 8^V$. Engineer this cascaded amplifier by choosing all six resistor values and the width of the MOS to meet all conditions. You are also allowed a large capacitor to short a resistor in AC. If you choose, indicate which one resistor. Conditions:

- $V_{OUT}/V_{IN} \geq 300$.

- $(W/L)_N$ should realistically be at least 20.

- To protect each transistor, neither stage should have an absolute gain of higher than 30.

- Maximum DC power consumption is 1 mW.

5) High Frequency Analysis of MOS Amplifiers

Given the amplifier below, where $\lambda = 0$, $V_{TH} = 0.4^V$, $\mu_N C_{OX} = 400\ \mu A*V^{-2}$, W/L = 30, $V_{BIAS} = 0.5^V$,

$R_D = 50^{k\Omega}$, and an L that (for part b and d) is super large so any AC signal will open circuit it,

a) Find the drain current in DC.

b) From the small signal model, find the low frequency gain V_{OUT}/V_{IN}.

c) Using your gain from part b), find the exact output and input impedance

in terms of L, C_{GD}, C_{DS}, C_{GS}, and ω. Do not open circuit the inductor.

d) Approximate the output pole frequency, if $4C_{GD} = 2C_{GS} = C_{DS} = 20$ fF.
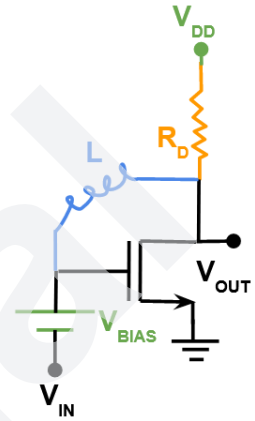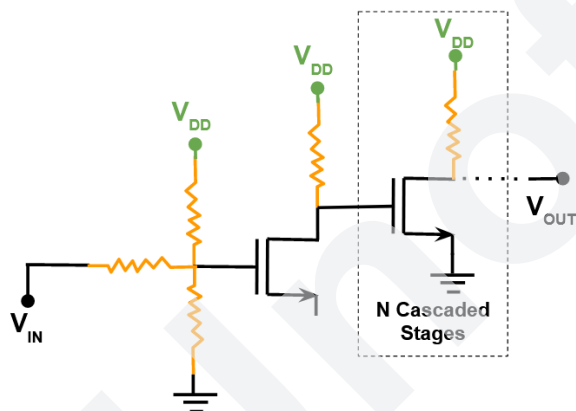
6) Feedback

For a negative feedback amplifier with forward gain of A and feedback gain of β,

$$A(s) = \frac{10^{13}}{(s+T_X)(s+10)(s+10^3)(s+10^5)}.$$

Find phase margin and comment on stability for each T_X and β combination below. If the open loop system is unstable, find an extra factor, K, of gain to A(s) so the open loop system oscillates.
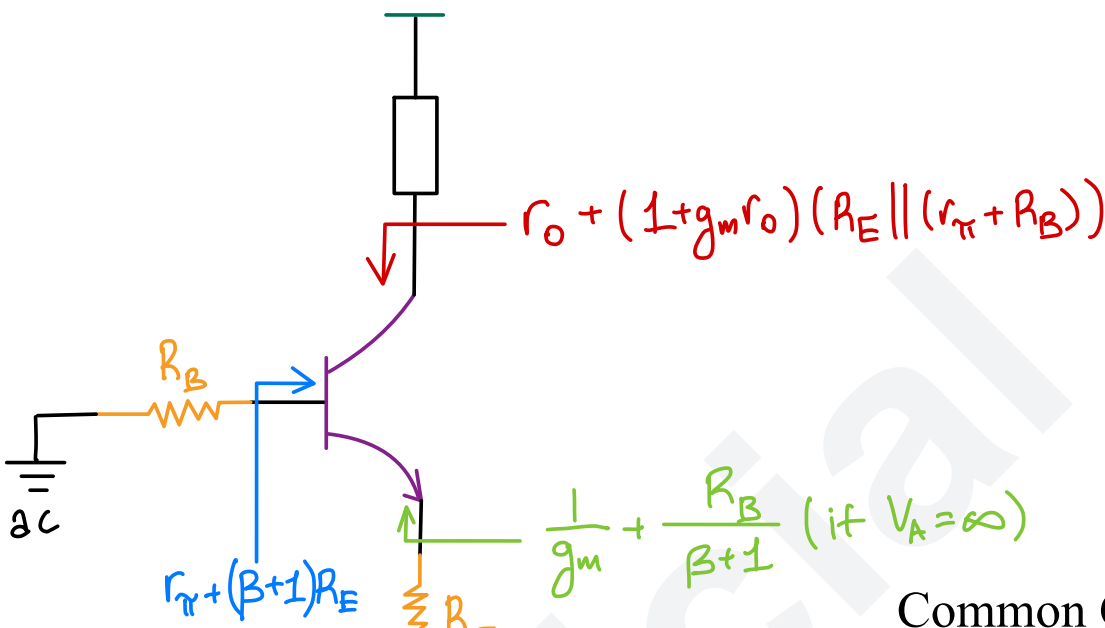
	T_X	β	PM (^{O}) - Stable?	Open Loop Stability	K (if applicable)
a)	1	1			
b)	10	0.1			
c)	0	0.01			

d) Given a general amplifier (not necessarily part a-c), complete the circuit using general

resistors to implement negative feedback. What (kind of) value should N be?
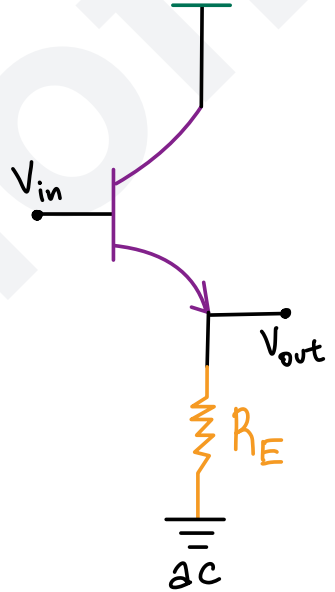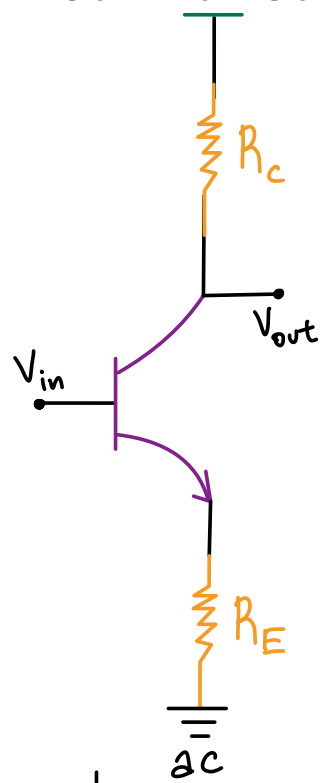
Topology Sheet

$$r_0 + (1 + g_m r_0)(R_E \| (r_\pi + R_B))$$

R_B

$r_\pi + (\beta+1) R_E$

$$\frac{1}{g_m} + \frac{R_B}{\beta+1} \quad (\text{if } V_A = \infty)$$

R_E

Common Base

R_c

V_{out}

V_B

R_E

V_{in}

$$\left. \frac{V_{out}}{V_{in}} \right| = \frac{R_c}{\frac{1}{g_m} + R_E} \quad V_A = \infty$$

Emitter Follower

V_{in}

V_{out}

R_E

$$\frac{V_{out}}{V_{in}} = \frac{R_E \| r_0}{\frac{1}{g_m} + R_E \| r_0}$$

Common Collector

R_c

V_{out}

V_{in}

R_E

$$\left. \frac{V_{out}}{V_{in}} \right| = \frac{-R_c}{\frac{1}{g_m} + R_E} \quad V_A = \infty$$